ADS1610EVM

This user's guide describes the characteristics, operation, and use of the ADS1610 16-bit, 10-MSPS high-speed, parallel interface, analog-to-digital converter evaluation board. A complete circuit description, a schematic diagram, and a bill of materials is included. Contact the Product Information Center or e-mail *dataconvapps@list.ti.com* for questions regarding this EVM.

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1.1 Features

- Full-featured evaluation board for the ADS1610 10-MSPS high-speed 16-bit, single-channel, parallel interface, delta sigma type analog-to-digital converter.
- Onboard signal conditioning
- Onboard reference, with recommended buffer circuitry
- Input and output digital buffers
- Basic system-level logic decoding.

2 Introduction

The ADS1610 is high-speed, high-resolution delta sigma (ΔΣ) analog-to-digital converter. It features a data rate of 10 MSPS and an advanced multistage analog modulator combined with an on-chip digital decimation filter. The ADS1610 achieves 86 dBFS signal-to-noise ratio (SNR) in a 5-MHz signal bandwidth. The device offers outstanding performance at these speeds with a total harmonic distortion of –94 dB. The ADS1610 ΔΣ topology provides key system-level design advantages with respect to antialias filtering and clock jitter. The design of the antialias filter is simplified because the on-chip digital filter greatly attenuates out-of-band signals. The ADS1601 filter has a *brick wall* response with a flat pass band (±0.0002 dB of ripple) followed immediately by a wide stop band (5 MHz to 55 MHz). Clock jitter becomes especially critical when digitizing high-frequency, large-amplitude signals. The ADS1610 significantly reduces clock jitter sensitivity by an effective averaging of clock jitter as a result of oversampling the input signal. Output data is supplied over a parallel interface and easily connects to TMS320 digital signal processors (DSP). The power dissipation can be adjusted with an external resistor, allowing for reduction at lower operating speeds. With its outstanding high-speed performance, the ADS1610 is well-suited for demanding applications in data acquisition, scientific instruments, test and measurement equipment, and communications.

The ADS1610EVM is a stand-alone, full-featured system that offers data-sheet performance. Additionally, the EVM conforms to a common electrical and mechanical pinout for digital I/O enabling it to be quickly adapted to various host platforms.

2.1 Analog Interface

The analog interface consists of the following subsections:

1. Analog input
2. External reference generation
3. Modulator clock

2.1.1 Analog Input Signal Conditioning

The ADS1610 measures the differential signal, VIN = (AINP-AINP), against the differential reference, VREF = (VREFP – VREFN). The analog input signal can be applied to the board through the SMA connectors J4 and J41. The board arrives with the input circuitry configured for single-ended in, differential output, as shown in Figure 1. It has a 50 -Ω termination; therefore, the signal source needs to be able to provide a 3 -V single-ended signal with this termination. The single-ended analog signal can be applied at J4.

The onboard input driver is designed using the wide-band, low-distortion, fully differential amplifier (THS4503) from Texas Instruments. The amplifier is configured for a gain of 2. The THS4503 can directly accept differential signals or be used to convert a single-ended input signal to a differential one. The factory-set condition is for a single-ended input converted to fully differential at the output of the THS4503. The desired output common-mode signal is fed through pin 2 of the THS4503. The required common mode is 2.5 V. This voltage is generated onboard in the reference voltage generation circuitry.

The ADS1610 has relaxed antialiasing filter requirements because it is a delta sigma converter. A simple antialiasing filter comprising a 24-Ω resistor and a 300- pF capacitor with a –3-dB bandwidth of 22 MHz is used at the output of the THS4503.

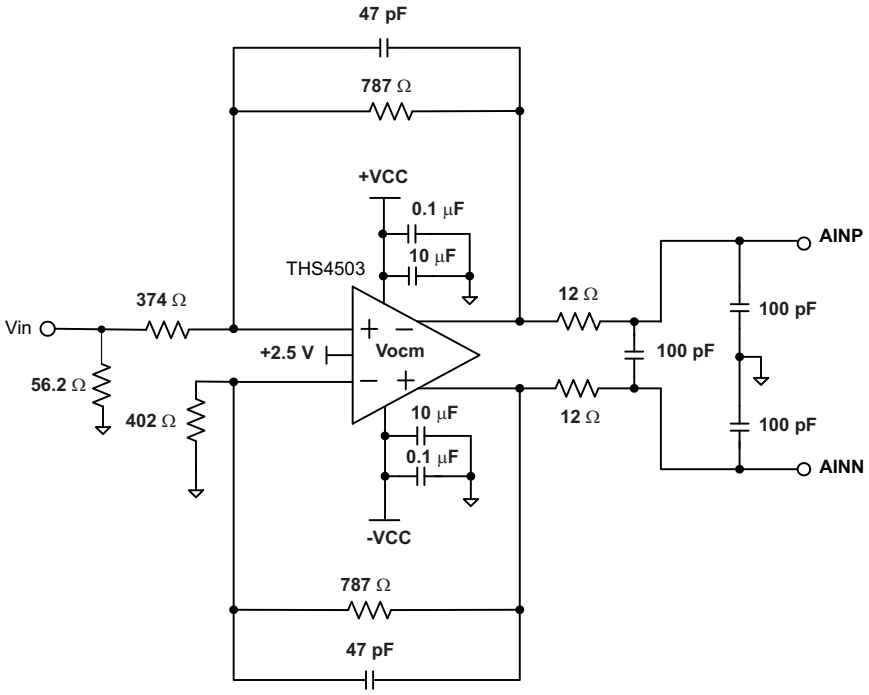


Figure 1. Input Circuitry

2.1.2 External Reference Generation

The ADS1610 operates from an external voltage reference. The reference voltage VREF is set by the differential voltage between VREFN and VREFP: VREF = (VREFP-VREFN). VMID must be 2.5 V.

The ADS1610EVM has onboard reference generation circuitry using the low-noise, high-speed THS4031 from Texas Instruments. Three of these amplifiers are used to generate the REFP (VREFP), CML (VMID) and REFM (VREFM) voltages. The CML voltage generated in this circuitry also is used as the common-mode voltage for the input driver (THS4503). The three reference voltages can be adjusted using the trim potentiometers R37, R38, and R40.

The reference voltage source for the onboard reference generation circuitry is selectable. If W1 jumper position is across pins 1 and 2, then AVDD1 is selected. When the jumper is placed across pins 2 and 3, the REF02 is selected as the source. The ADS1610EVM leaves the factory with a short across pins 2 and 3 of W1.

The factory-set voltages are 4 V, 2.5 V, and 1 V for VREFP, VCML, and VREFM, respectively. These voltages provide a reference voltage of 3 V single-ended. The ADS1610 with a 3-V reference can achieve an SNR of 86 dBFS in the 0 – 5-MHz bandwidth.

If the application requires a smaller reference voltage, then potentiometers R37 and R38 can be adjusted to generate the desired voltage. Be aware that there is a tradeoff between SNR and reference voltages. Table 1 gives the reference voltage versus SNR tradeoff.

Table 1. Reference Voltages

Reference	VREFM	VCML	VREFP	Peak In-Band SNR
3 V	1	2.5	4	86
2.5 V	1.25	2.5	3.75	85
2 V	1.5	2.5	3.5	83

For more information on the reference generation circuitry, see sheet 6 of the ADS1610EVM schematic, at the end of this user's guide.

2.1.3 Clock Source

The ADS1610 uses the external clock signal applied to the CLK input pin as the modulator clock. Input sampling is controlled by this clock signal. As with any high-speed data converter, a high-quality clock is essential for achieving optimum performance. In order to maximize SNR performance of the converter, keep the jitter on this clock source below those recommended in the ADS1610 data sheet.

The modulator clock can be fed into the ADS1610 from two sources. It can be applied via SMA connector (J4) or from the onboard source. The onboard source is the 60-MHz oscillator installed at X1. The factory-set condition applies the onboard 60-MHz oscillator to the CLK pin of the ADS1610. The user-supplied external clock must be fed to the board through the SMA connector, J4. The board has a footprint at R9 for a 50 -Ω termination on this line. It can be installed at the user's discretion. If R9 is not installed by the user and the user clock is generated from a 50-Ω source, then be sure to reduce the clock amplitude to half.

To switch from the onboard oscillator to the user clock applied at J4, change the position of jumper of W3 from pins 1–2 to 2–3.

The performance of the ADS1610 is sensitive to clock jitter; see the data sheet for the requirements.

Table 2. Jumper Setting

Reference Designator	1-2	2-3	Description
W1	Installed(1)	Not installed	Set voltage on AVDD1 as source for the reference generation circuitry.
	Not installed	Installed	Set voltage REF02 as the source for the reference generation circuitry.
W2	Installed(1)	Not installed	Enable 60-MHz oscillator
	Not installed	Installed	Disable 60-MHz oscillator
W3	Installed(1)	Not installed	Set modulator clock to onboard 60-MHz oscillator
	Not installed	Installed	Set modulator clock to user-supplied clock via J4.

(1) Factory installed

3 Digital Interface

This section describes the digital sections and pinout of the ADS1610EVM.

3.1 Board-Level Control

3.1.1 DIP Switch Options

Optional settings for the ADS1610 are set and controlled manually via a DIP switch – SW1. The functions controlled by this switch are summarized in Table 3.

Table 3. Switch Function Control, SW1

Switch, SW1			
Position	**Function**	**ON(LO)**	**OFF(HI)**
1	Mode 0 pin	Set M0 to 0	Set M0 to 1
2	Mode 1 pin	Set M1 to 0	Set M0 to 1
3	Power-down bit	Device is powered down	Device is not powered down
4	Not used		
5	Not used		
6	Not used		

Table 3. Switch Function Control, SW1 (continued)

Switch, SW1			
Position	**Function**	**ON(LO)**	**OFF(HI)**
7	Not used		
8	Not used		

3.1.2 Jumper Options

Four jumpers are associated with the digital control section; their functions are detailed in Table 4.

Table 4. Digital Jumper

Reference Designator	1-2	2-3	Description
W20	Installed	Not installed	Set SYNCB to output of combinatory logic
	Not installed	Installed(1)	Set SYNCB to user reset switch
W23	Installed(1)	Not installed	Set DRDY_OUT to DRDY of ADS1610
	Not installed	Installed	Set DRDY_OUT to inverted DRDY of ADS1610.
J19 2-1	Installed(1)	N/A	Set U16A pin 2 to LOW. Used in EVM address decoding logic.
J19 3-4	Installed(1)	N/A	Set U17A pin 2 to LOW. Used in board address decoding logic.

(1) Factory installed

3.1.3 ADS1610EVM OTR LED

When the analog input exceeds the positive full-scale value or goes below negative full-scale value of VREF, the Out of Range (OTR) signal goes HIGH and remain high while the signal is out-of-range. When this condition occurs, LED1 illuminates. To clear the LED, flip-flop U13 must be reset. Depending on which position W20 is set to, the LED can be reset manually via SW2 or through programming by issuing a WR operation from the host processor. The factory-set condition of W20 is a short across pins 2-3. This allows the user to manually reset the LED and reset the ADS1610.

3.1.4 ADS1610 Reset

The ADS1610 can be asynchronously reset when the SYNC pin is driven low. In reset, all the digital circuits are cleared, the data bus is LOW, and DRDY is HIGH. The ADS1610 can be reset in two ways, using an manual reset via SW1 or by programming from the host system. If W20 pins 1-2 are shorted, the SYNC signal must be generated by the host system. If W20 pins 2-3 are shorted, then the SYNC signal to the ADS1610 is generated manually by momentarily depressing switch SW2.

3.1.5 Interrupt Source

Some microprocessors only recognize falling edge interrupts; others only recognize rising edge interrupts. Some can be programmed to recognize either. W23 can be set by the user to select either rising edge or falling edge. If a jumper is across pins 1 and 2, DRDY is applied to DRDY_OUT pin. If jumper short is across pins 2 and 3, an inverted version of DRDY is applied to DRDY_$\overline{\text{OUT}}$ pin.

3.1.6 Base Address and Chip Select

The EVM can be mapped into a memory location by setting a base address. The EVM has four possible base addresses. The base address is set by J19. When the logic state of the two external address signals matches the logic state set up by the two jumpers on J19 and the access is valid memory access, the EVM generates a $\overline{\text{CS}}$ signal for the ADC. This then can be further qualified as a read cycle or a write (RESET) cycle. An installed jumper is equivalent to logic 0 on the corresponding address line. An uninstalled jumper is equivalent to logic 1 on the corresponding address line.

The TMS320C6713 DSK provides two memory spaces for the daughterboards. The two memory spaces enables (CE2 and CE3) are buffered versions of the DSP outputs and are not generated by decode logic on the DSK. The 5-6K EVM uses CE2 to indicate that the access is valid. The places the daughterboard at an address space beginning at 0xA0000000.

Table 5. Memory Space Address

J19		Address Selected
1-2	3-4	
0	0	0xA0000000
0	1	0xA0000004
1	0	0xA0000008
1	1	0xA000000C

3.2 External Interface

The pinout for the ADS1610EVM has been arranged to easily mate with the growing range of interface adapters. The interface board that is currently available is the 5-6K Interface Board (see SLAU104). This board enables any TMS320C5000 DSP platform or TMS320C6000 DSP platform-based DSK with standard expansion connectors to connect to the EVM.

3.3 Data Connector Pinout

The data from the ADC is available at J18 and at J2. J18 is available for interfacing to 5-6K interface board, user breadboard, or ribbon cable. Connector J2 is installed to allow users to connect the ADS1610EVM directly to the TSW1100 data capture board (see SLAU164) from Texas Instruments. The application section of this user's guide explains how an ADS1610 can be evaluated using the TSW1100 and ADS1610EVM.

The pin assignments and function of each of the pins on J2 and J18 are given in Table 6 and Table 7.

Table 6. Assignment and Function at J18

Description	Signal	Connector Pin	Connector Pin	Description
Buffered data bit 0 (LSB)	D0	J18.1	J18.2	Ground
Buffered data bit 1	D1	J18.3	J18.4	Ground
Buffered data bit 2	D2	J18.5	J18.6	Ground
Buffered data bit 3	D3	J18.7	J18.8	Ground
Buffered data bit 4	D4	J18.9	J18.10	Ground
Buffered data bit 5	D5	J18.11	J18.12	Ground
Buffered data bit 6	D6	J18.13	J18.14	Ground
Buffered data bit 7	D7	J18.15	J18.16	Ground
Buffered data bit 8	D8	J18.17	J18.18	Ground
Buffered data bit 9	D9	J18.19	J18.20	Ground
Buffered data bit 10	D10	J18.21	J18.22	Ground
Buffered data bit 11	D11	J18.23	J18.24	Ground
Buffered data bit 12	D12	J18.25	J18.26	Ground
Buffered data bit 13	D13	J18.27	J18.28	Ground
Buffered data bit 14	D14	J18.29	J18.30	Ground
Buffered data bit 15	D15	J18.31	J18.32	Ground
	N/C	J18.33	J18.34	Ground
	N/C	J18.35	J18.36	Ground
	N/C	J18.37	J18.38	Ground

Table 6. Assignment and Function at J18 (continued)

Description	Signal	Connector Pin	Connector Pin	Description
	N/C	J18.39	J18.40	Ground

Table 7. Assignment and Function at J2

Description	Signal	Connector Pin	Connector Pin	Signal	Description
Ground	Ground	J2.1	J2.2	N/C	
Ground	Ground	J2.3	J2.4	N/C	
Ground	Ground	J2.5	J2.6	D0	Buffered data bit 0 (LSB)
Ground	Ground	J2.7	J2.8	D1	Buffered data bit 1
Ground	Ground	J2.9	J2.10	D2	Buffered data bit 2
Ground	Ground	J2.11	J2.12	D3	Buffered data bit 3
Ground	Ground	J2.13	J2.14	D4	Buffered data bit 4
Ground	Ground	J2.15	J2.16	D5	Buffered data bit 5
Ground	Ground	J2.17	J2.18	D6	Buffered data bit 6
Ground	Ground	J2.19	J2.20	D7	Buffered data bit 7
Ground	Ground	J2.21	J2.22	D8	Buffered data bit 8
Ground	Ground	J2.23	J2.24	D9	Buffered data bit 9
Ground	Ground	J2.25	J2.26	D10	Buffered data bit 10
Ground	Ground	J2.27	J2.28	D11	Buffered data bit 11
Ground	Ground	J2.29	J2.30	D12	Buffered data bit 12
Ground	Ground	J2.31	J2.32	D13	Buffered data bit 13
Ground	Ground	J2.33	J2.34	D14	Buffered data bit 14
Ground	Ground	J2.35	J2.36	D15	Buffered data bit 15
Ground	Ground	J2.37	J2.38	**N/C**	
Ground	Ground	J2.39	J2.40	**DRDY_OUT**	

3.3.1 Control Connector Pinout

The ADC is controlled by the signals that originate from J10/P10. The assignment and function of each pin is given in Table 8.

Table 8. Assignment and Function at J10/P10

Description	Signal	Connector Pin	Connector Pin	Signal	Description
Chip Select signal from host processor	HOST_CSa(1)	J10.1	J10.2	GROUND	
Write signal from host processor	HOST_WR	J10.3	J10.4	GROUND	
Read signal from host processor	HOST_RD(1)	J10.5	J10.6	GROUND	
	N/C	J10.7	J10.8	GROUND	
	N/C	J10.9	J10.10	GROUND	
Address signal from host processor	HOST_A2(1)	J10.11	J10.12	GROUND	
Address signal from host processor	HOST_A3(1)	J10.13	J10.14	GROUND	
Out of Range signal	OTR_INT	J10.15	J10.16	GROUND	
		J10.17	J10.18	GROUND	
Data Ready or inverted Data Ready signal	DRDY_OUT	J10.19	J10.20	GROUND	

(1) Factory-set condition is to short these signals to ground.

The ADS1610EVM arrives with CS, HOST_RD, HOST_A2, and HOST_A3 signals set LOW. This enables the ADS1610 and at power up allows the device to start converting. The modes pins (M0 and M1) are factory set to enable a data rate of 10 MHz.

4 Power Supplies

The ADS1610EVM board requires various power sources for operation.

- A dual ±7-Vdc supply for best performance of the analog front end and reference generation circuitry. These voltages can be applied at J11.
- Two +5-Vdc supplies for the ADS1610 analog supply and clock supply. Apply 5 V at J12 and J13.
- A single +3-Vdc supply for digital section of the board (A/D + address decoder + buffers). Apply 3 V to J1.

5 Using the EVM

The ADS1610EVM serves two purposes. It functions as an evaluation/development board and a reference design.

5.1 Development/Evaluation Board

The two common methods used to evaluate the ADS1610EVM's performance are:

1. EVM used as a stand-alone system. The user is responsible for capturing and analyzing the data, typically via a logic analyzer and analysis software (LABView, MATLAB, etc.).
2. EVM used with TI's TSW1100 data capture board solution:
   http://focus.ti.com/docs/toolsw/folders/print/tsw1100.html

5.1.1 EVM and TSW1100 Capture Board

The user's guide for the data capture board (SLAU164) provides detailed information and setup instructions.

The ADS1610EVM mates with the TSW1100 board via J2. Two data ports are available on the data capture board; the reference designators are J1 and J2. Figure 2 shows the ADS1610 plugged into the TSW1100 board.

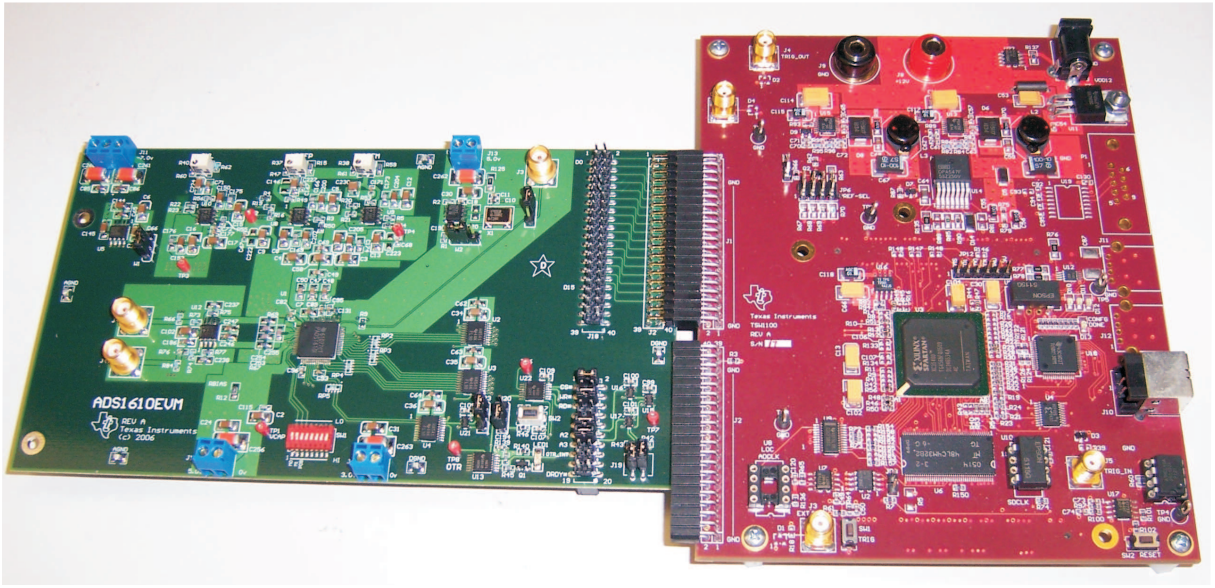


Figure 2. TSW1100 and ADS1610EVM Setup

Figure 3 is a screen shot of the TSW1100 front panel.

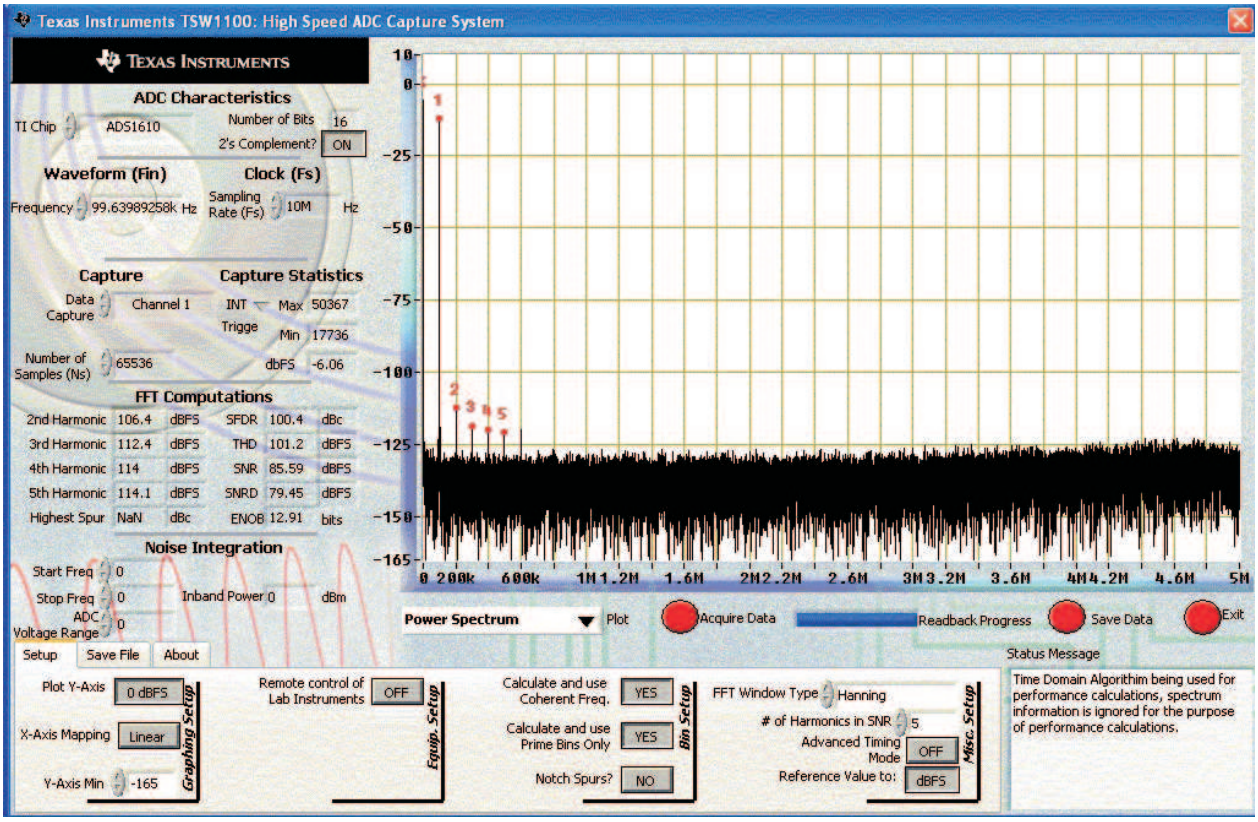


Figure 3. TSW1100 Screen Shot

Using the TSW1100 software, perform the following steps.

1. Select ADS1610 from the TI Chip pulldown menu.
2. Set Sampling Rate : 10 MHz (if modulator clock is 60-MHz oscillator)
3. Set Waveform (Fin) frequency to test frequency; then set ARB to the frequency shown in this field.
4. Select *Channel 1* from the Data Capture Selector pulldown menu. If it appears grayed out, select another channel, and then select channel 1. It should appear enabled.
5. Set data samples to 65536 from default 16384
6. Select Power Spectrum from the PLOT pulldown menu.
7. Set FFT Window Type to *NONE*.
8. Click Acquire Data. After data is captured and processed, check to see if dBFS field reads approximately –6 dB. If not, adjust the signal amplitude, and then click Acquire Data. Do this until dBFS is approximately –6dB.
9. Once the signal amplitude is 6 dB less FS, select Hanning from the FFT Window Type.
10. Notice SFDR, THD, and SNR. The results should be similar to those shown in the following figures.

Figure 4 through Figure 8 are typical test results at different input frequencies using an Valpey Fisher oscillator (60 MHz) and the TSW1100 data capture board. The analog input signal is from a HP 33120A ARB and was band-pass filtered before being applied to J4 on the ADS1610EVM.

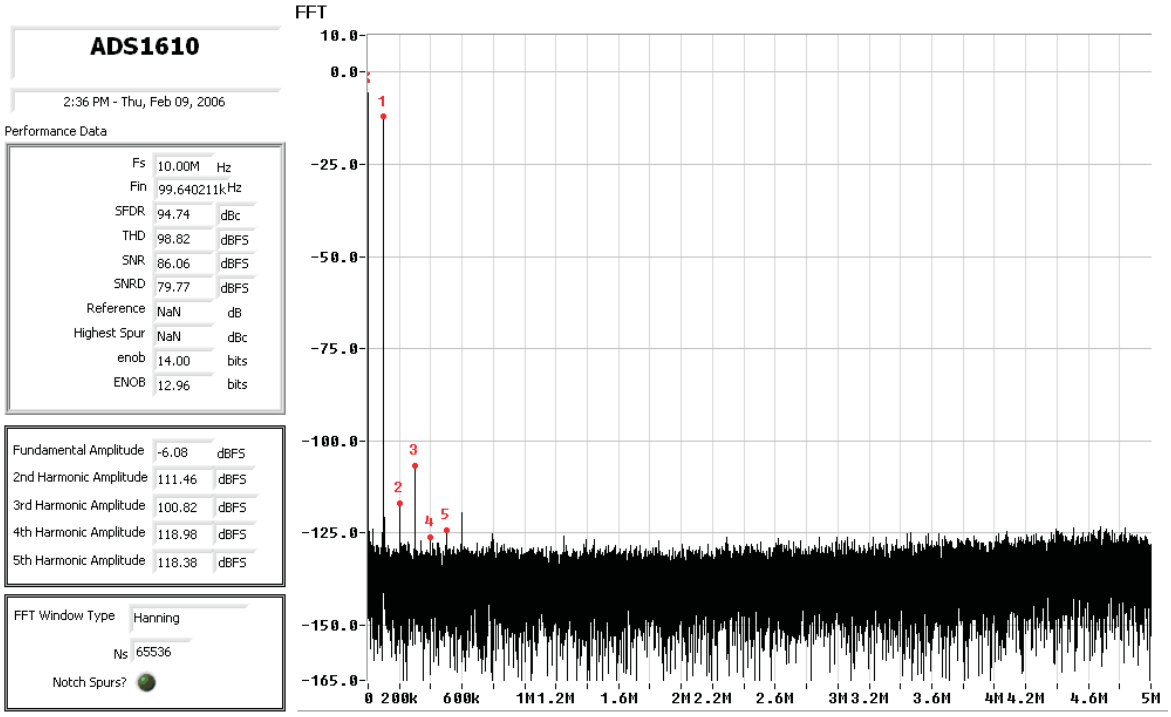


Figure 4. Test Results With a 100-kHz Input Frequency

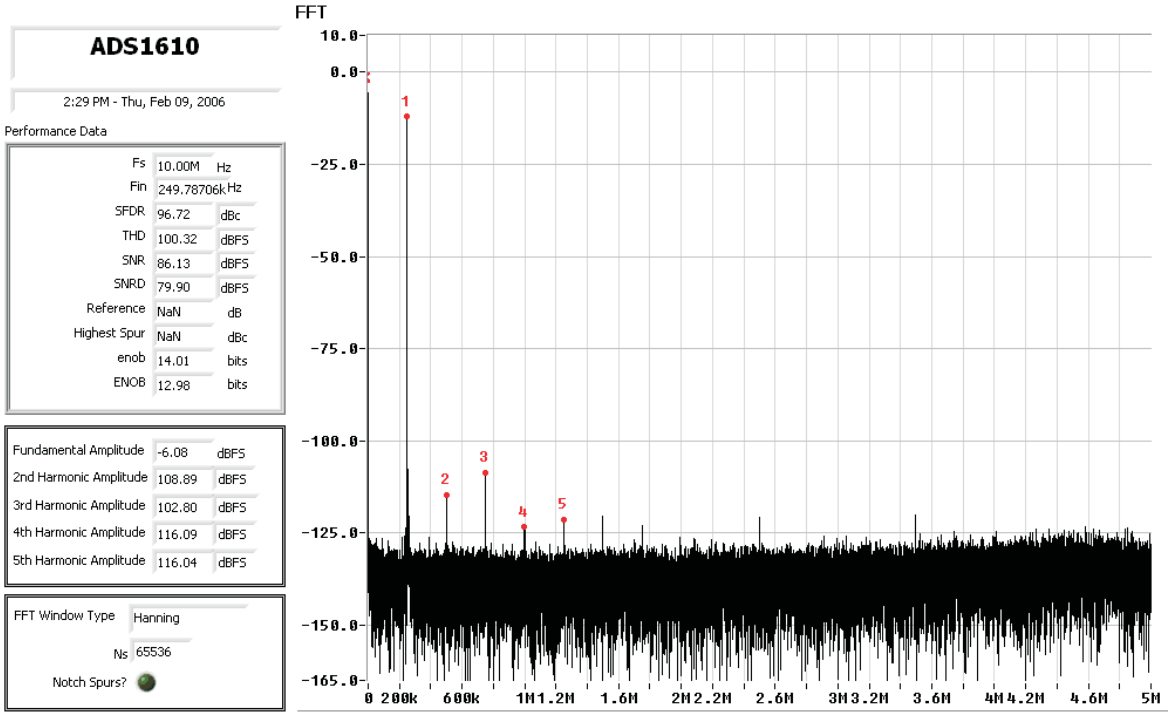


Figure 5. Test Results With a 250-kHz Input

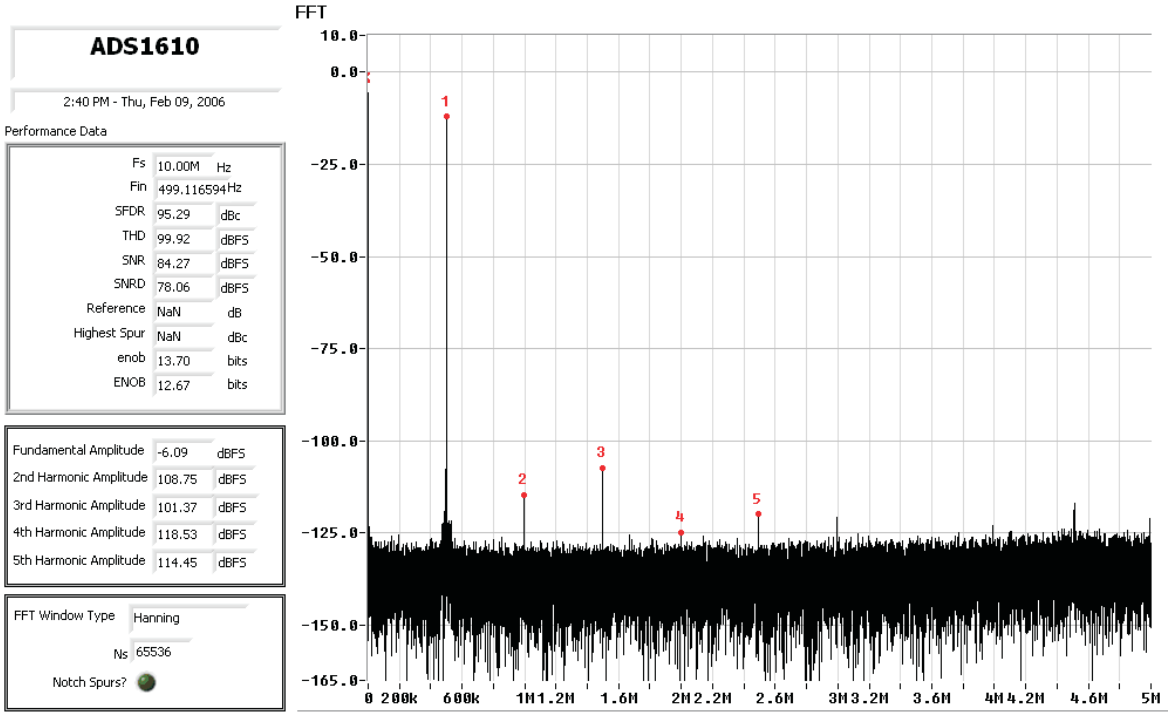


Figure 6. Test Results With a 500-kHz Input

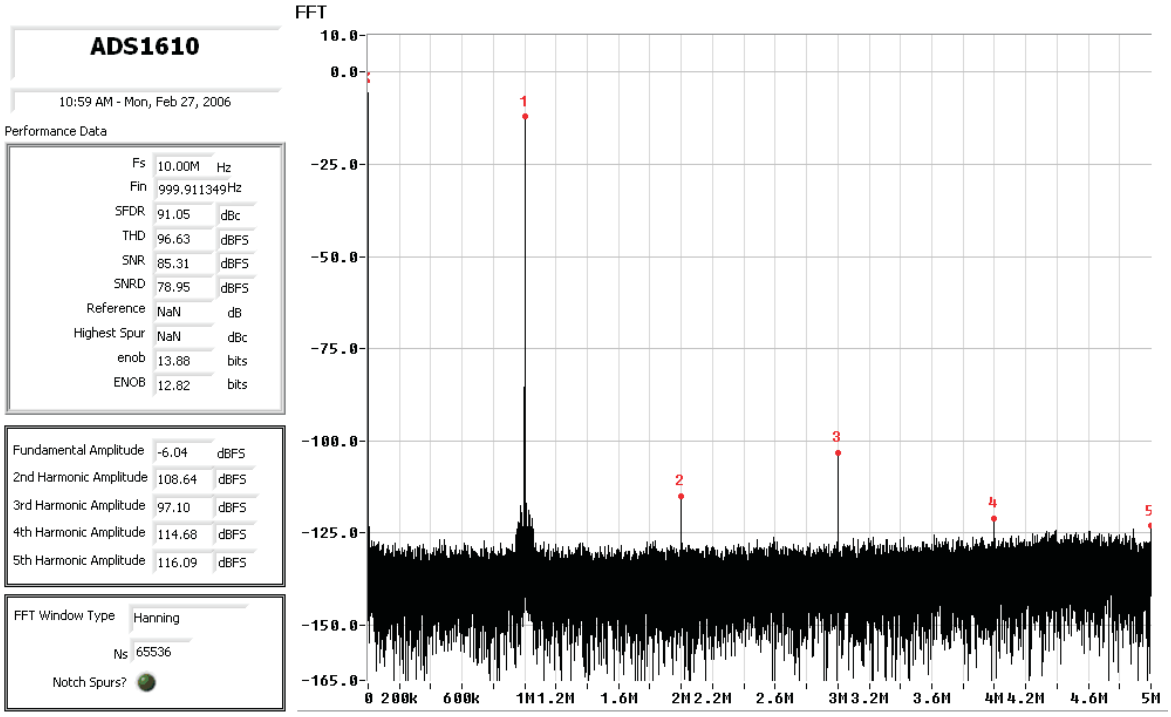


Figure 7. Test Results With a 1-MHz Input

At higher input frequencies, SFDR is sensitive to the quality of the modulator clock. Therefore, if using an external clock source, be sure it is a high-quality, low-jitter clock source that is used to drive the modulator clock.

Referring to the 1-MHz and 2-MHz test cases, the spurs around the fundamental is the noise floor of the signal source showing through the pass band of the filter. The band-pass filter sufficiently attenuates the noise in the stop band.

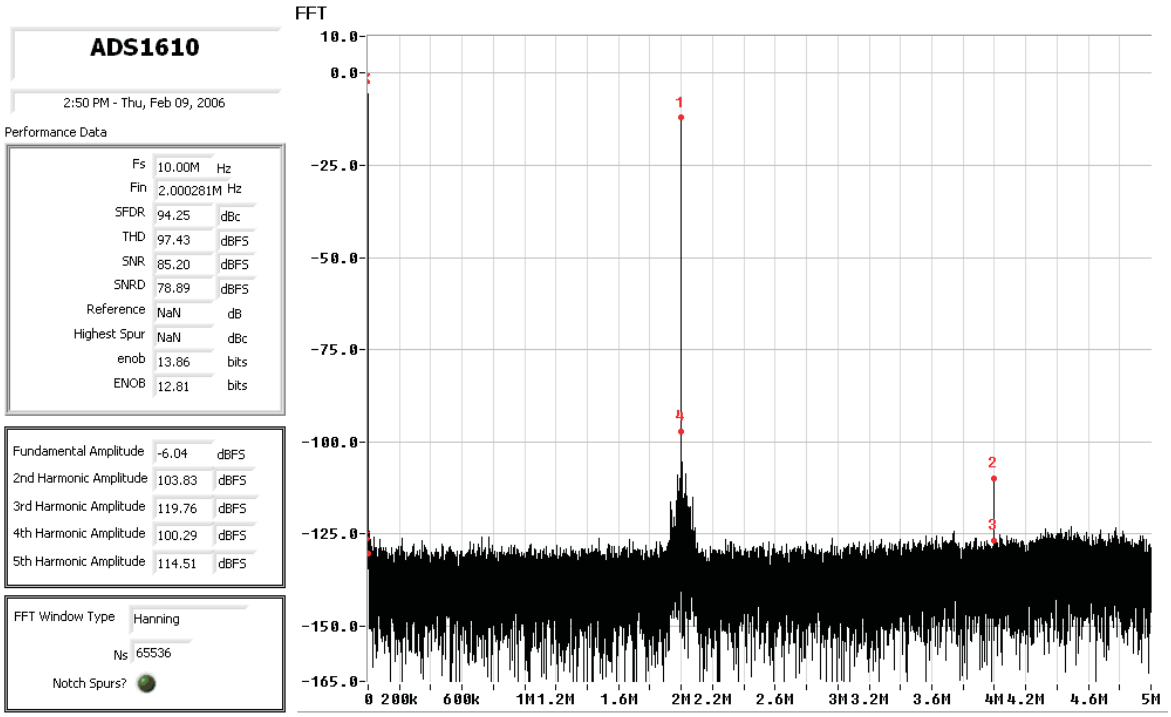


Figure 8. Test Results With a 2-MHz Input

Three approaches can be used to perform development activity:

1. EVM used with TI DSK (e.g., TMS320C6713 DSK) and 5-6K interface board. No custom software exists to analyze the data captured by the DSP.
2. EVM used with one of many development kits supported by AVNET and *Texas Instruments Analog Adapter Kit*. Ensure that the development kit supports AVNET's AVbus standard; you can navigate to the AVNET Web site at http://www.em.avnet.com/evk/home and find the Analog Adapter kit along with various third-party development kits.
3. Design and build your own custom interface.

5.2 Reference Design

The ADS1610EVM is a reference design for the ADS1610. It provides a real-world model for the hardware engineer tasked to integrate the ADS1610 onto the user system board. To achieve the best performance, the layout used on the ADS1610EVM should be replicated as much as possible. The layout and component placement of the reference circuitry and modulator clock are critical for achieving best performance. It is recommended that the modulator clock be routed under the chip and up to the CLK pin. The 60-MHz high-frequency clock should be routed as far away from the reference and input circuitry as possible before being routed to the chip. It is vitally important that the reference and power supply pins be well bypassed near the pins of the device.

The bill of materials and schematic pages for the ADS1610EVM are in the appendixes at the end of this document.

6 Related Documentation from Texas Instruments

To obtain a copy of any of the following TI documents, call the Texas Instruments Literature Response Center at (800) 477-8924 or the Product Information Center (PIC) at (972) 644-5580. When ordering, identify this booklet by its title and literature number. Updated documents can also be obtained through The TI Web site at www.ti.com.

Data Sheets	**Literature Number:**
ADS1610	SBAS344
REF02	SBVS003
REG101	SBVS026
SN74AHC1G04	SCLS318
SN74AHC1G32	SCLS317
SN74AHC1G86	SCLS323
SN74AHC32	SCLS247
SN74AHC74	SCLS255
SN74AHC541	SCLS261
THS4031	SLOS224
THS4503	SLOS352

Appendix A Bill of Materials

The following table contains a complete Bill of Materials for the EVM. The schematic diagram is also provided for reference. Contact the Product Information Center or e-mail dataconvapps@list.ti.com for questions regarding this EVM.

Qty	Value	Reference Designators	Footprint	Manufacturer	Manufacturer's Part Number	Description
5	0	T1–T5	1210	Keystone Electronics	5015	PC Test point miniature SMT
4	0	R3 R4 R5 R50 R54 R55	0603	Yageo America	9C06031A0R00JLHFT	RES 0.0 Ω 1/10W 5% 0603 SMD
1	10R0	R125	1206	Yageo America	9T12062A10R0FBHFT	RES 10.0 Ω 1/8W 1% SMD
2	12R4	R67 R69	0603	Yageo America	9T06031A12R4FBHFT	RES 12.4 Ω 1/10W 1% SMD
5	33R	RP1–RP5	CTS_742_4RES	CTS Corporation Resistor/Electrocomponents	742C083330JTR	RES Array 33 Ω 8TERM 4RES SMD
2	56.2R	R66 R84	0603	Yageo America	9T06031A56R2FBHFT	RES 56.2 Ω 1/10W 1% SMD
1	49.9R	R9	0603	Not Installed	Not Installed	
6	100R	R49 R53 R56	0603	Yageo America	9T06031A1000FBHFT	RES 100 Ω 1/10W 1% SMD
6	332R	R16 R19–R23	0603	Yageo America	9T06031A3320FBHFT	RES 332 Ω 1/10W 1% SMD
2	374R	R73 R76	0603	Yageo America	9T06031A3740FBHFT	RES 374 Ω 1/10W 1% SMD
1	374R	R76	0603	Not Installed	Not Installed	
1	402R	R74	0603	Yageo America	9T06031A4020FBHFT	RES 402 Ω 1/10W 1% SMD
2	787R	R75 R77	0603	Yageo America	9T06031A7870FBHFT	RES 787 Ω 1/10W 1% SMD
1	1.24K	R60	0603	Yageo America	9T06031A1241FBHFT	RES 1.24 kΩ 1/10W 1% SMD
1	2.15K	R62	0603	Yageo America	9T06031A2151FBHFT	RES 2.15 kΩ 1/10W 1% SMD
3	5K	R37 R38 R40	Bourns_3224W	Bourns Inc	3224W-1-502E	TRIMPOT 5 kΩ 4mm TOP ADJ SMD
2	7.50K	R47 R61	0603	Yageo America	9T06031A7501FBHFT	RES 7.50 kΩ 1% SMD
6	10K	R1 R2 R42 R43 R45 R139	0603	Yageo America	9T06031A1002FBHFT	RES 10.0 kΩ 1/10W 1% SMD
1	10K	RP14	CTS_742_8RES	CTS Corporation Resistor/Electrocomponents	742C163103JTR	RES Array 10 kΩ 16TRM 8RES SMD
2	12.4K	R15 R59	0805	Yageo America	9C08052A1242FKHFT	RES 12.4 kΩ 1/8W 1% SMD
1	19K	R12	0805	Yageo America	9C08052A1912FKHFT	RES 19.1 kΩ 1/8W 1% SMD
1	130K	R147	0603	Yageo America	9T06031A1303FBHFT	RES 130 kΩ 1/10W 1% SMD
1	150R	R140	0603	Yageo America	9T06031A1500FBHFT	RES 150 Ω 1/10W 1% SMD
1	169K	R46	0603	Yageo America	9T06031A1693FBHFT	RES 169 kΩ 1/10W 1% SMD
9	1000pF	C124–C127 C130–C134	0402	TDK Corporation	C1005X7R1H102K	CAP CER 1000PF 50V X7R 10%
4	0.1µF	C44 C77 C81 C91	0402	TDK Corporation	C1005X5R1A104K	CAP CER 0.10 µF 10V X5R 10%
5	1000pF	C115–C118 C129	0603	TDK Corporation	C1608C0G1H102J	CAP CER 1000 PF 50V C0G 5%
17	0.1 µF	C66 C11 C18 C19 C78 C82 C89 C93 C95 C96 C99 C100 C101 C107–C109 C194	0603	TDK Corporation	C1608X7R1C104K	CAP CER 0.10 µF 16V X7R 10%
1	10 µF	C7	0805	TDK Corporation	C2012X5R0J106M	CAP CER 10 µF 6.3V X5R 20% 0805
19	0.1 µF	C62–C65 C85–C88 C90 C173– C176 C166 C169 C186 C246 C247	0805	TDK Corporation	C2012X7R1E104K	CAP CER 0.10 µF 25V X7R 10%

Qty	Value	Reference Designators	Footprint	Manufacturer	Manufacturer's Part Number	Description
1	0.1 µF	C76	1206	TDK Corporation	C3216X7R2A104K	CAP CER 0.1 µF 100V X7R 10%
10	1 µF	C10 C206–C214	0603	TDK Corporation	C1608X5R1C105K	CAP CER 1.0 µF 16V X5R 10%
3	1 µF	C47 C48 C50	0805	TDK Corporation	C2012X5R1A105K	CAP CER 1.0 µF 10V X5R 10%
5	1 µF	C141–C145	1206	TDK Corporation	C3216X7R1H105K	CAP CER 1 µF 50V X7R 10%
1	2.2 µF	C221	1206	TDK Corporation	C3216X7R1C225K	CAP CER 2.2 µF 16V X7R 10%
1	10 µF	C230	1210	TDK Corporation	C3225X5R1A106K	CAP CER 10 µF 10V X5R 10%
14	10 µF	C2 C6 C21 C22 C24 C30 C31 C34–C36 C58 C102 C224 C227	1206	TDK Corporation	C3216X5R1A106M	CAP CER 10 µF 10V X5R 20%
5	47 µF	C256 C260–C263	1210	Panasonic - ECG	ECJ-4YB1C476M	CAP Ceramic 47 µF 16V X5R
2	47 pF	C237 C238	0603	TDK Corporation	C1608C0G1H470J	CAP CER 47 pF 50V C0G 5%
3	100 pF	C253–C255	0805	TDK Corporation	C2012C0G1H101J	CAP CER 100 pF 50V C0G 5%
3	NI	C43 C45 C46	0402	NOT INSTALLED	NOT INSTALLED	*
6	NI	C67 C68 C72 C171 C177 C167	0603			
4	NI	C20 C49 C69 C71	0805	TDK Corporation	C2012C0G1H103J	
17	NI	C3–C5 C8 C9 C12 –C17 C150 C152 C200 C202 C204 C205	1206			
1	NI	C146	1210	Not Installed	Not Installed	*
2	NI	C222 C223	3216	Not Installed	Not Installed	*
5	NI	C1 C39–C42	3528	Not Installed	Not Installed	*
1		U1	64-TQFP (PWP) Modified	Texas Instruments	ADS1610IPAPR	16-Bit, 10MSPS Delta-Sigma analog-to-digital Converter
1	NI	U5	8-SOP(D)	Not Installed	Not Installed	IC +5V Voltage reference 8-SOIC
1		U6	SO-8	Texas Instruments	REG101UA-3.3	IC LDO Regulator 3.3V 100 mA 8SOP
1		U21	DBV(R-PDSO-G5)	Texas Instruments	SN74AHC1G04DBVR	IC single inverter gate SOT23-5
1		U15	DBV(R-PDSO-G5)	Texas Instruments	SN74AHC1G32DBVR	IC SGL 2IN POS-OR Gate SOT23-5
2		U16 U17	DBV(R-PDSO-G5)	Texas Instruments	SN74AHC1G86DBVR	IC SGL 2IN EX-OR Gate SOT23-5
1		U22	14-TSSOP(PW)	Texas Instruments	SN74AHC32PWR	IC quad 2-IN POS-OR Gate 14TSSOP
1		U13	14-TSSOP(PW)	Texas Instruments	SN74AHC74PWR	IC dual EDG-TRG DTYP F-F 14TSSOP
3		U2–U4	20-TSSOP(PW)	Texas Instruments	SN74AHC541PWR	Octal Buffers/Drivers with 3-state outputs
3		U8–U10	SO-8	Texas Instruments	THS4031ID	IC 100 MHz LN V-FDBCK AMP 8-SOIC
1		U12	8-SOP(D)	Texas Instruments	THS4503CD	High-Speed Fully-Differential Amplifiers
3		J1 J12 J13	OST_ED1514	On Shore Technology	ED555/2DS	Terminal block 3,5 mm 2POS PCB
1		J2	20X2X.1	Samtec	TSW-120-11-T-D-RA	Right Angle 20 pin connector
1		J18	20X2X0.1_SMT_ PLUG_&_SOCKET	Samtec	SSW-120-22-S-D-VS	0.025 SMT Socket - bottom side of PWB
1				Samtec	TSM-120-01-T-D-V-P	0.025" SMT PLUG - Top side of PWB
1		J11	OST_ED1515	On Shore Technology	ED555/3DS	Terminal block 3.5 mm 3POS PCB
3		J3 J4 J41	SMA_JACK	Emerson Network Power Connectivity Solutions	142-0701-206	CONN Recept straight PCB 0.155" NI
1		J10	10X2X.1_SMT_PLUG_&_SOCKET	Samtec	SSW-110-22-S-D-VS	0.025" SMT Socket - bottom side of PWB
1			40-Pin header	Samtec	TSM-110-01-T-D-V-P	0.025" SMT Plug - top side of PWB
1		J19	2X2X0.1_SMT	Samtec	TSM-102-01-T-DV	2 x 2 x 0.1 SMT Square Post Header
5		W1–W3 W20 W23	3 pos_jump	Samtec	TSW-103-07-L-S	3-position jumper
7		TP1–TP4 TP6–TP8	Through-hole test point	Keystone Electronics	5000	Test point PC MINI 0.040" D RED

Qty	Value	Reference Designators	Footprint	Manufacturer	Manufacturer's Part Number	Description
1		SW1	8-POS SMT Dip switch	ITT Industries	TDA08H0SK1	Switch DIP 8POS Half pitch SMT
1		SW2	EVQ-PJ	Panasonic	EVQ-PJU04K	Switch LT TOUCH 6x3.5 240GF SMD
1		LED1	LED-1206	Chicago Miniature Lamp Co.	CMD15-21VRC/TR8	Red LED
1		X1	OSC_CTS_SMT	Vapley Fisher Corporation	VF1SH-1-60.0MHz or VF900538-60.000 MHz	Oscillator, 60MHz Low Jitter
1		Q1	SOT23-3	Infineon	SMBT3904E6327	TRANS NPN 40V SOT-23

Appendix B Layout and Schematic

This appendix contains the EVM layout and schematic.

B.1 Layout

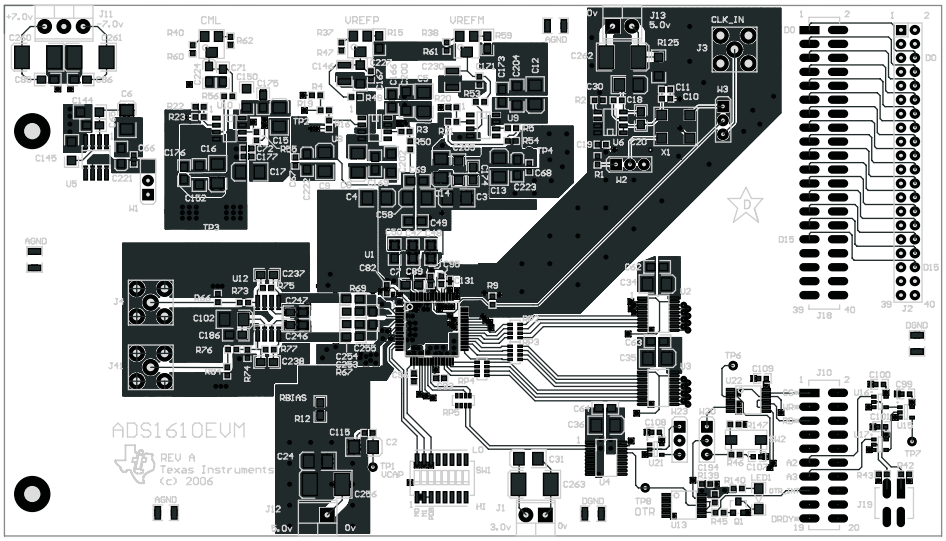


Figure B-1. Top Layer – Layer 1

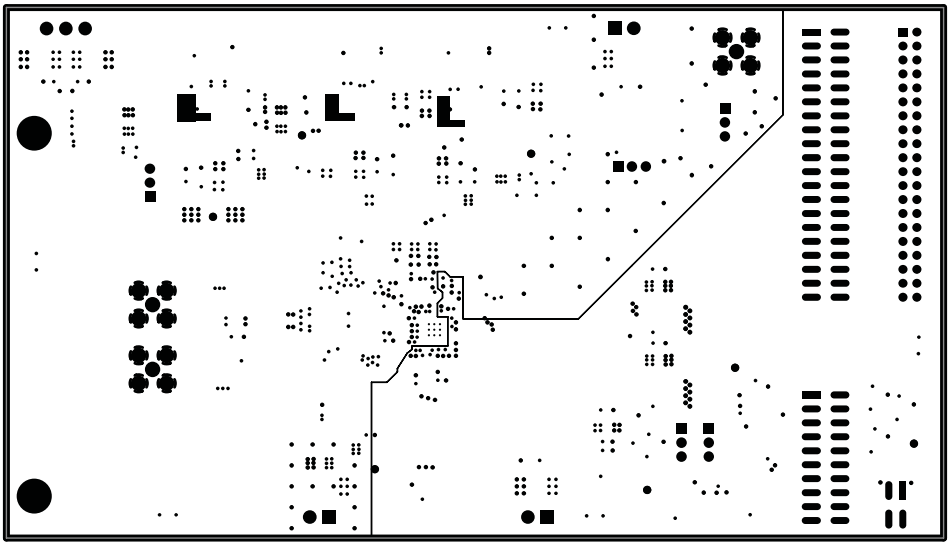


Figure B-2. Split Ground Plane – Layer 2

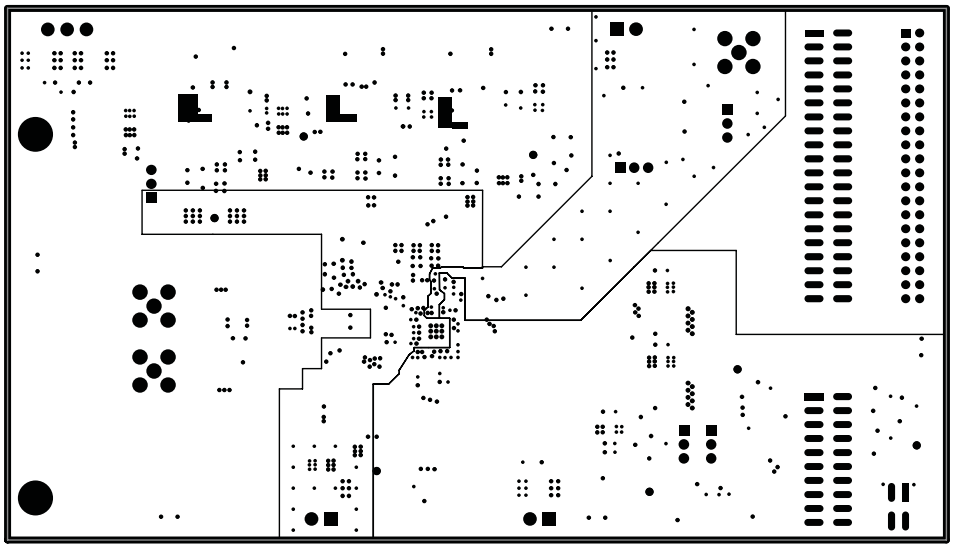


Figure B-3. Split Power Plane – Layer 3

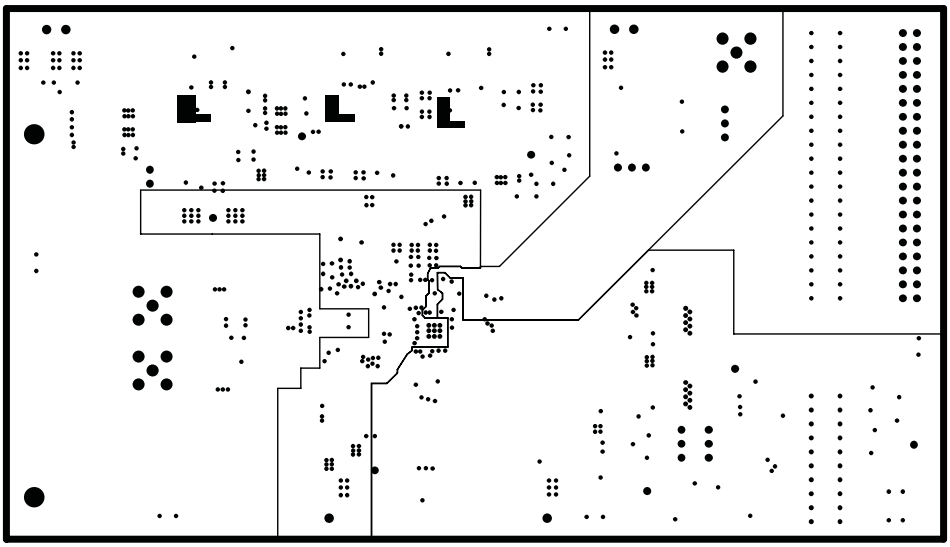


Figure B-4. Split Power Plane – Layer 4

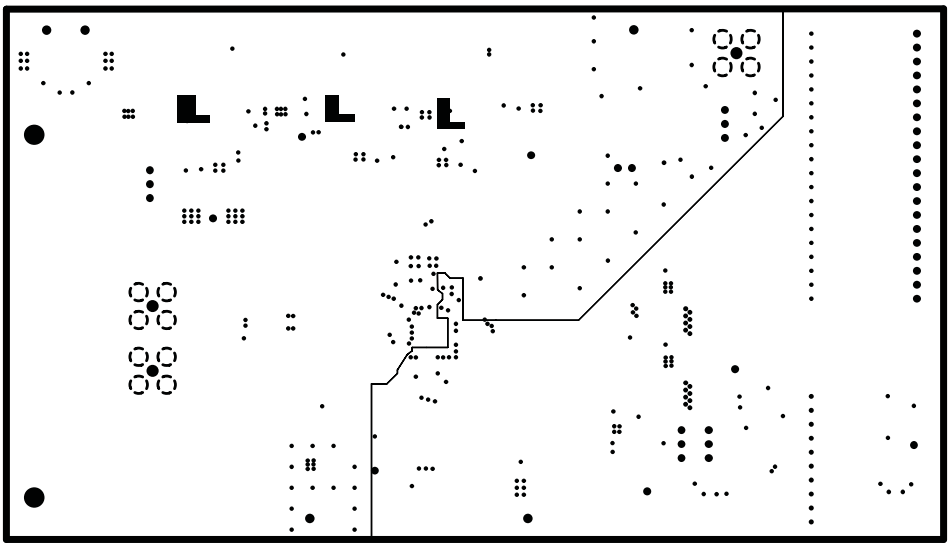


Figure B-5. Split Ground Plane – Layer 5

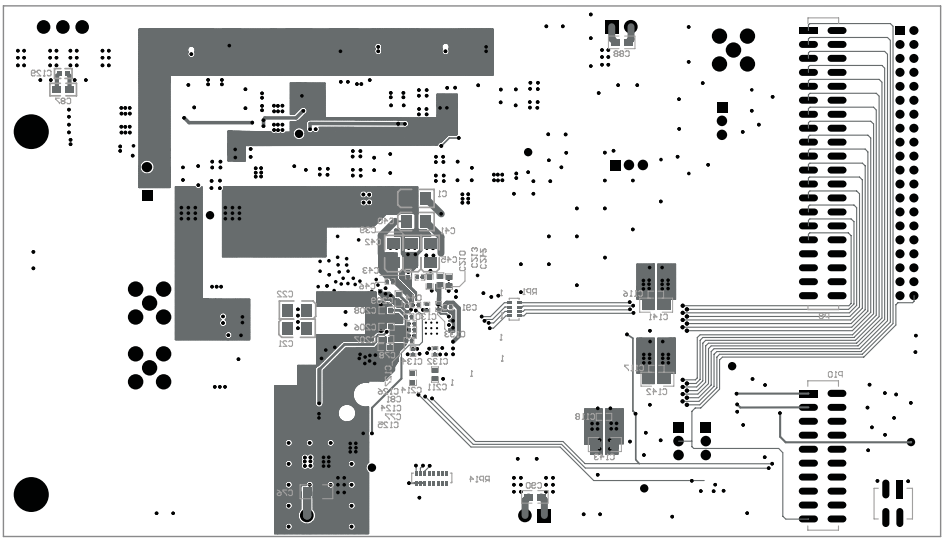


Figure B-6. Bottom Layer – Layer 6

B.2 Schematic

The ADS1610EVM schematic is appended to this page.

Revision History		
REV	ECN Number	Approved

ADS1610.Sch

Data bus buffers.Sch

Interface.Sch

Power.Sch

Diff Analog Input.Sch

Voltage Reference.Sch

TEXAS INSTRUMENTS

12500 TI Boulevard. Dallas, Texas 75243

Title: ADS1610 Block Diagram

Engineer: Joe Purvis			
Drawn By: Joe Purvis			
FILE: Block Diagram.sch	DOCUMENTCONTROL # 6455110		REV: A
	DATE: 18-Aug-2006	SIZE:	SHEET: 1 OF: 7

Revision History		
REV	ECN Number	Approved

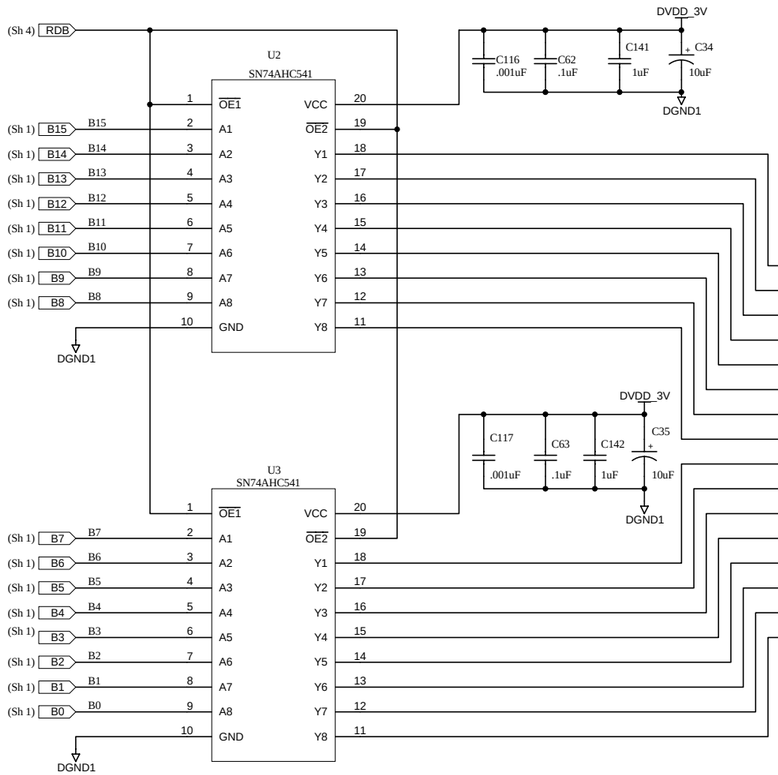
NOTES:

1. DO NOT INSTALL

Engineer: Joe Purvis	
Drawn By: Joe Purvis	
FILE: ADS1610.Sch	
Title: ADS1610	
DOCUMENTCONTROL # 6455110	REV: A
DATE: 18-Aug-2006	SIZE: SHEET: 2 OF: 7

TEXAS INSTRUMENTS
12500 TI Boulevard. Dallas, Texas 75243

Revision History		
REV	ECN Number	Approved



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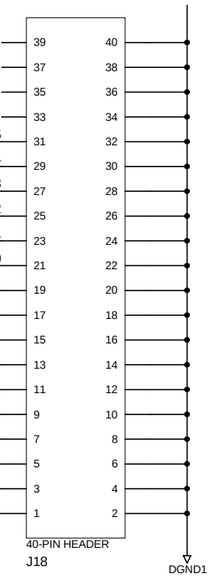
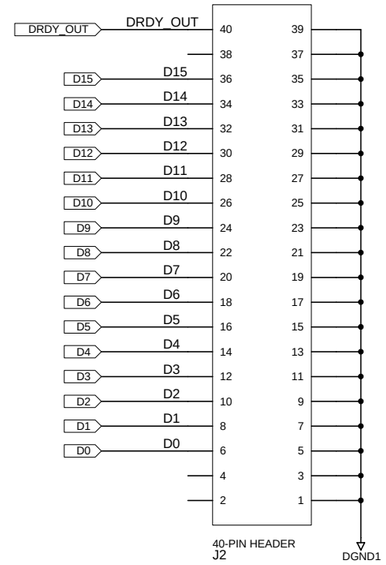
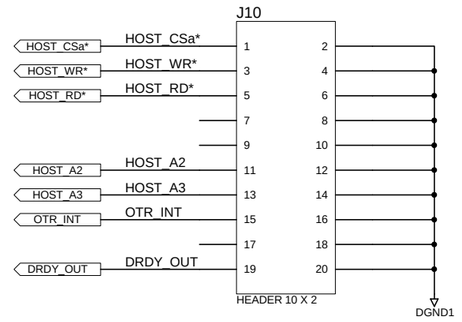


TSW1100





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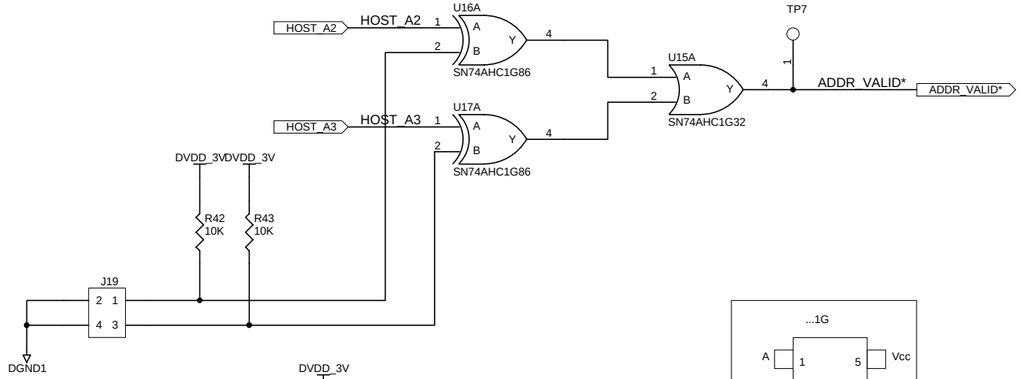
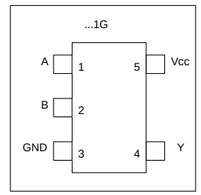
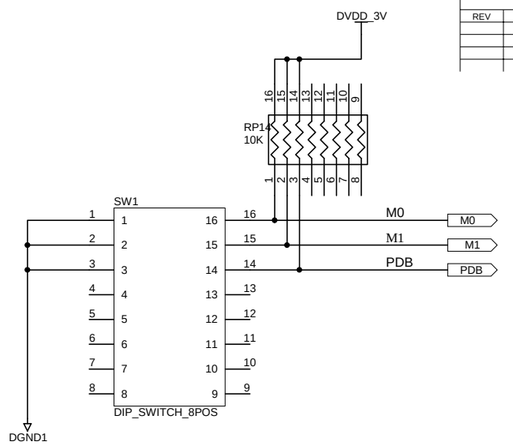
12500 TI Boulevard. Dallas, Texas 75243

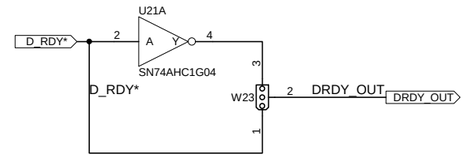
Title: Data bus buffers			
DOCUMENTCONTROL # 6455110			REV: A
Engineer: Joe Purvis	DATE: 18-Aug-2006	SIZE:	SHEET: 3 OF: 7
Drawn By: Joe Purvis			
FILE: Data bus buffers.Sch			

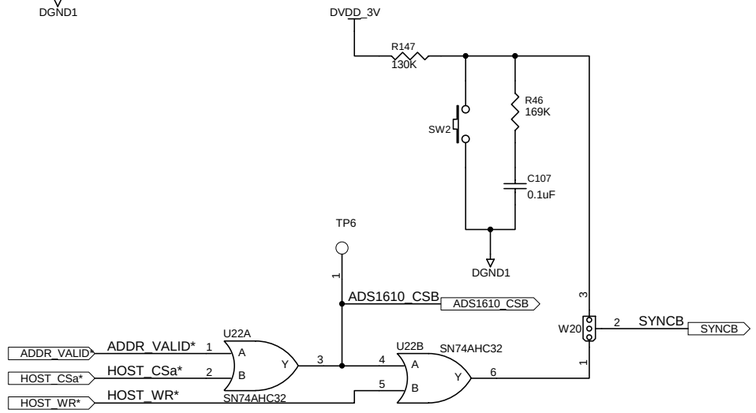
Revision History		
REV	ECN Number	Approved

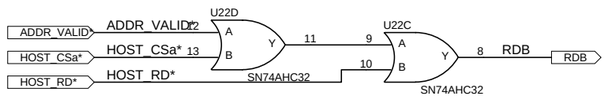


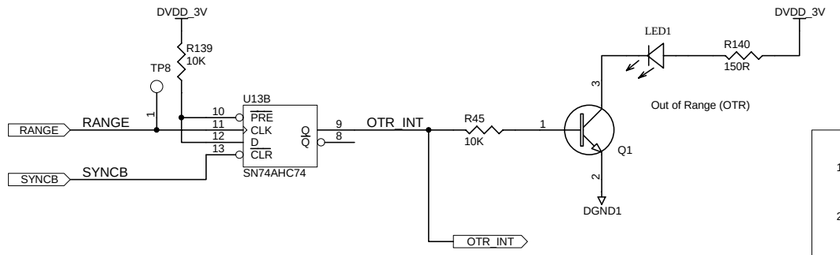


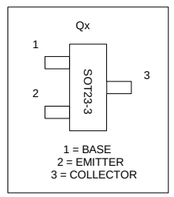


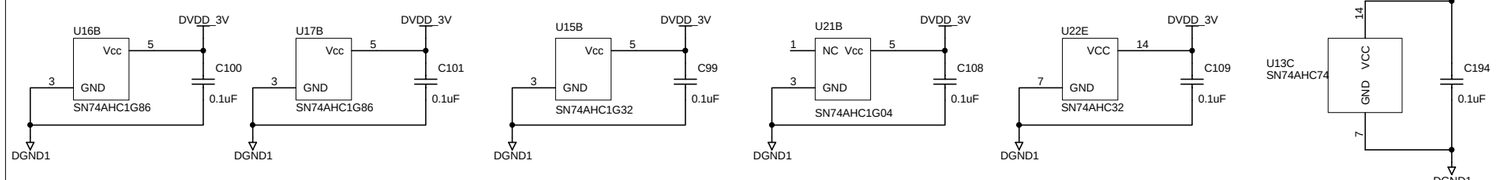












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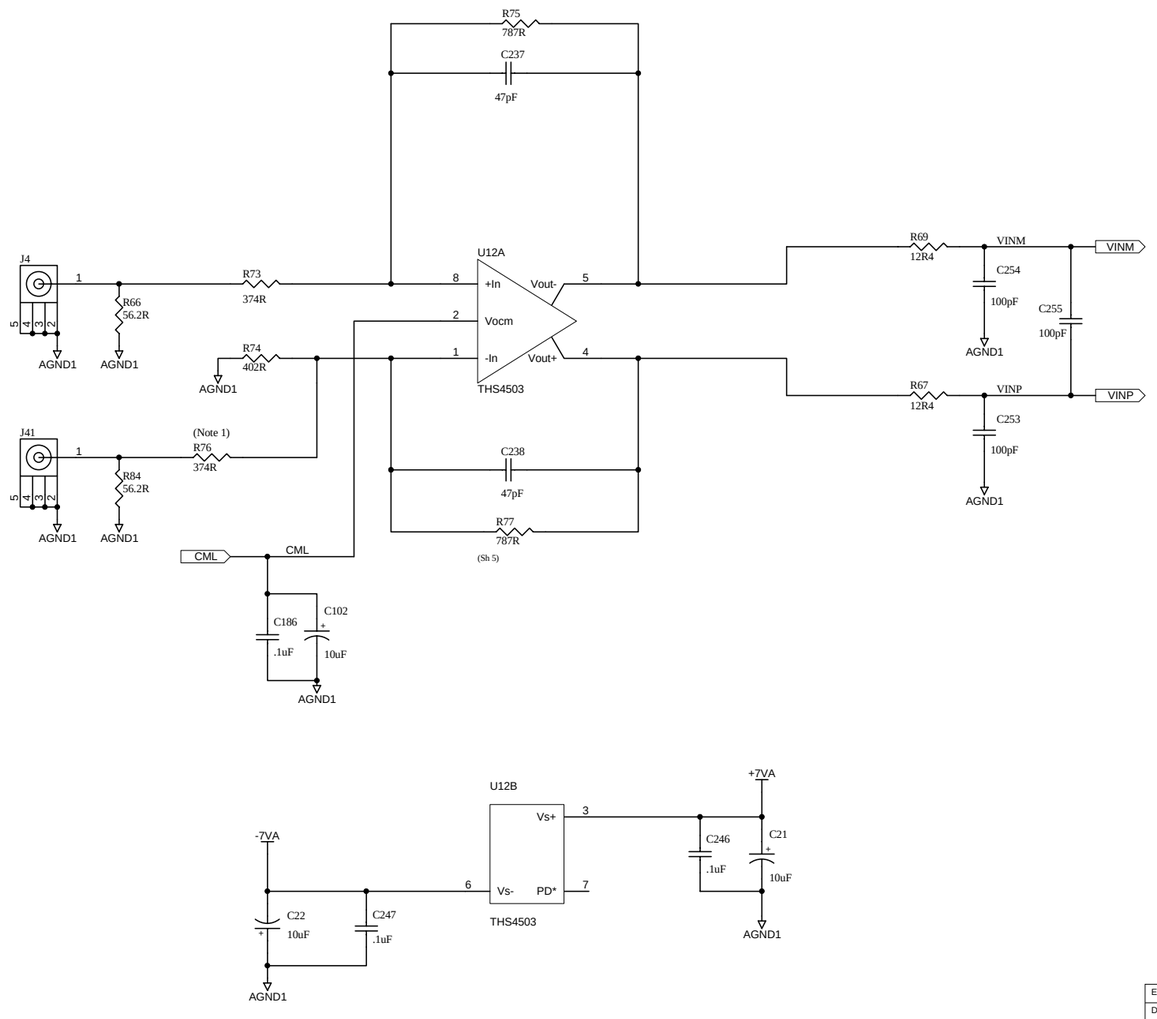
12500 TI Boulevard. Dallas, Texas 75243

Title: Interface			
DOCUMENTCONTROL # 6455110			REV: A
Engineer: Joe Purvis			
Drawn By: Joe Purvis			
FILE: Interface.Sch	DATE: 18-Aug-2006	SIZE:	SHEET: 4 OF: 7

Revision History		
REV	ECN Number	Approved



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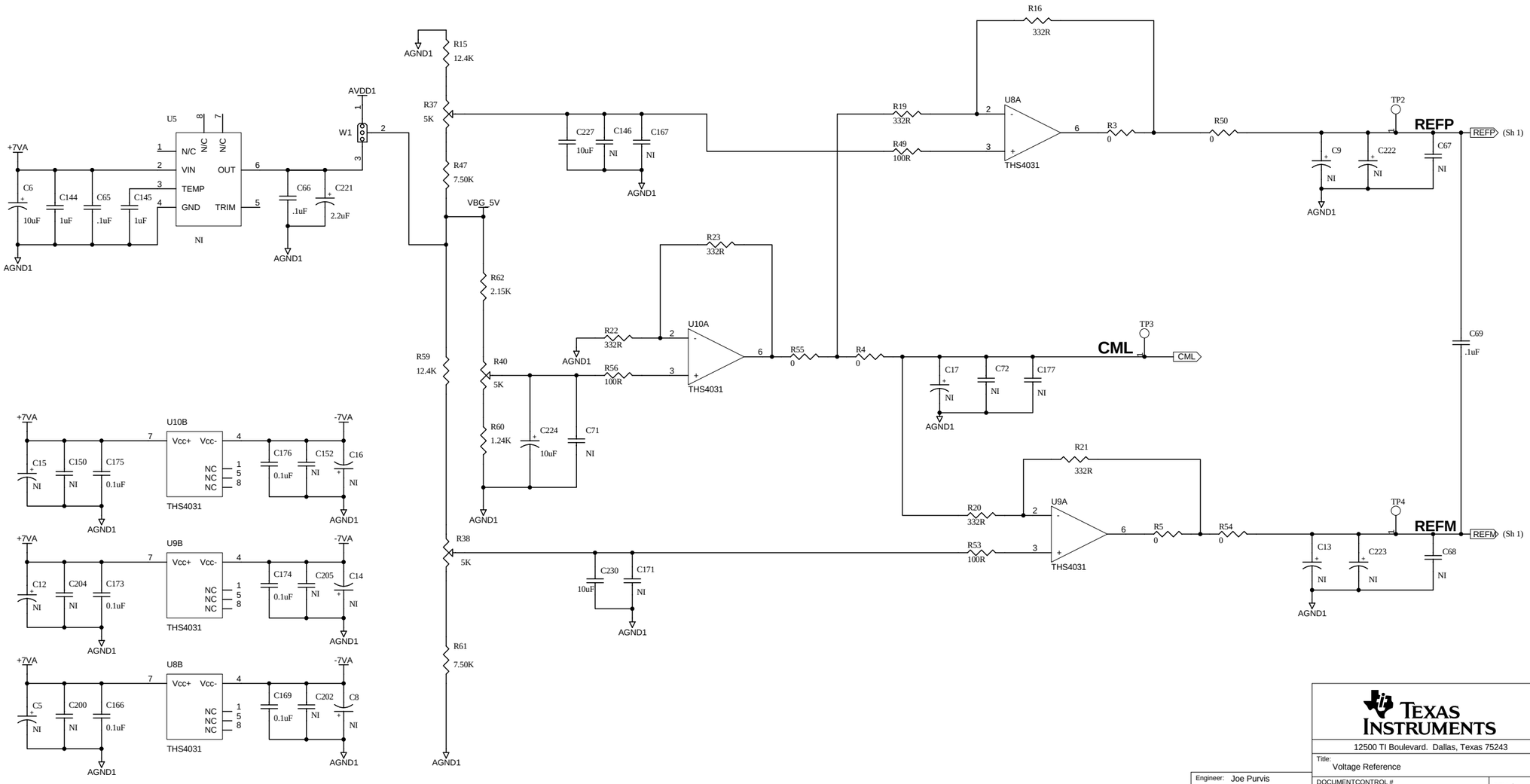
12500 TI Boulevard. Dallas, Texas 75243

Title: Diff Analog Input			
DOCUMENTCONTROL # 6455110			REV: A
DATE: 18-Aug-2006	SIZE:	SHEET: 5	OF: 7
Engineer: Joe Purvis			
Drawn By: Joe Purvis			
FILE: Diff Analog Input.Sch			

Revision History		
REV	ECN Number	Approved



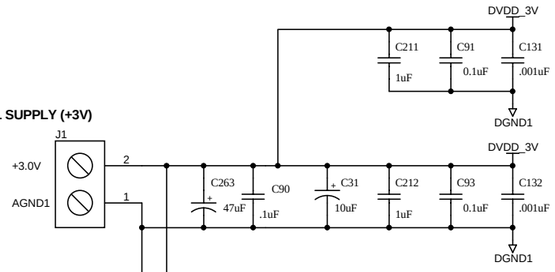
Engineer:	Joe Purvis
Drawn By:	Joe Purvis
FILE:	Voltage Reference.Sch

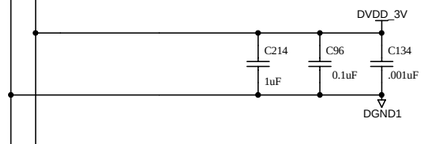
TEXAS INSTRUMENTS
12500 TI Boulevard. Dallas, Texas 75243

Title: Voltage Reference			
DOCUMENTCONTROL # 6455110			REV: A
DATE: 18-Aug-2006	SIZE:	SHEET 6	OF: 7

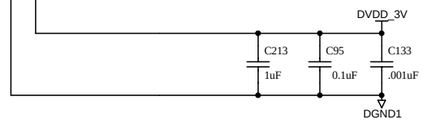
Revision History		
REV	ECN Number	Approved

ADC DIGITAL SUPPLY (+3V)



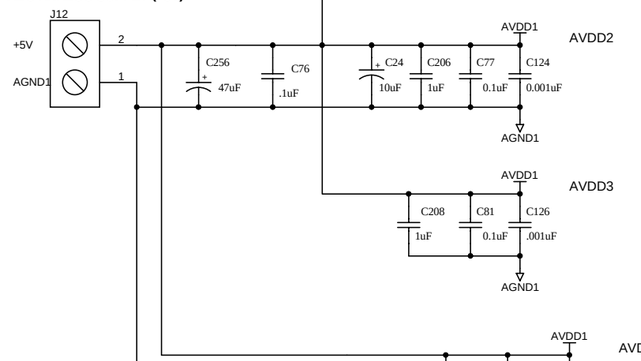


ADC COMP. SUPPLY (+3.0V)

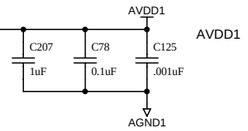


ADC OUTPUT DRIVER SUPPLY

ADC ANALOG SUPPLY (+5V)

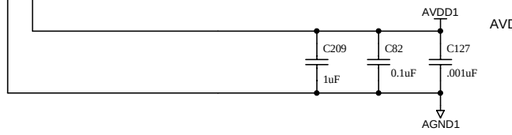


AVDD1



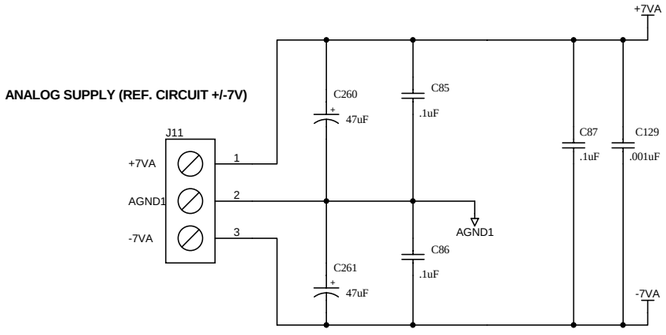
AVDD2

AVDD3

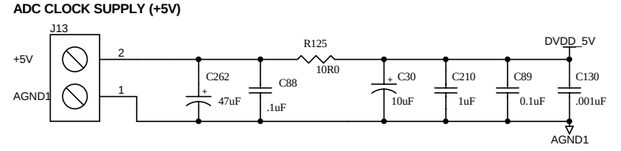


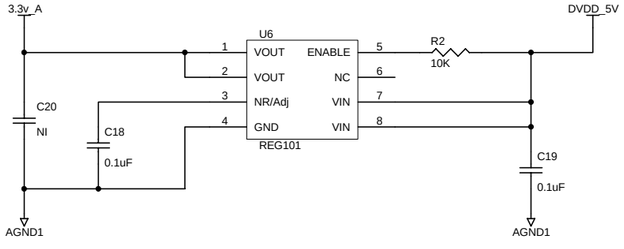
AVDD_REF

ANALOG SUPPLY (REF. CIRCUIT +/-7V)



ADC CLOCK SUPPLY (+5V)





TEXAS INSTRUMENTS

12500 TI Boulevard. Dallas, Texas 75243

Title: Power			
DOCUMENTCONTROL # 6455110			REV: A
DATE: 18-Aug-2006	SIZE:	SHEET: 7	OF: 7
Engineer: Joe Purvis			
Drawn By: Joe Purvis			
FILE: Power.Sch			

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of 6 V to 25 V and the output voltage range of 0 V to 5 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 60°C. The EVM is designed to operate properly with certain components above 60°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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